

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Priority Application Serial No. 09/438,310
Priority Filing Date November 10, 1999
Inventor Mark A. Helm et al
Assignee Micron Technology, Inc.
Priority Group Art Unit 2814
Priority Examiner S. Rao
Attorney's Docket No. MI22-2478
Title: Gated Semiconductor Assemblies and Methods of Forming Gated
Semiconductor Assemblies

INFORMATION DISCLOSURE STATEMENT
PURSUANT TO 37 C.F.R. §§ 1.56, 1.97 AND 1.98

In compliance with 37 C.F.R. §§ 1.56, 1.97 and 1.98, your attention is directed to the United States patents and other references listed on the attached Form PTO-1449. No admission is made regarding whether all the submitted references are prior art.


The listed references were cited by, or submitted to, the Office in the parent, co-pending application of the above-identified application. The above-identified application is a continuation application of co-pending application Serial No. 09/438,310, filed November 10, 1999. Such prior disclosure is sufficient for the above-identified application as far as copies of the references are concerned. 37 C.F.R. § 1.98(d) and MPEP § 609(2).

Citation of these references is respectfully requested.

Respectfully submitted,

Dated: 30 Jan 2004

By: _____


James E. Lake
Reg. No. 44,854

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| Form PTO-1449 | | U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE | | ATTY. DOCKET NO. MI22-2478 | Priority SERIAL NO. 09/438,310 | |
| LIST OF ART CITED BY APPLICANT (Use several sheets if necessary) | | | | APPLICANT Mark A. Helm | | |
| | | | | Priority FILING DATE November 10, 1999 | | Priority GROUP 2814 |
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| *Examiner Initial | Document Number | Date | Name | Class | Subclass | Filing Date If Appropriate |
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| | AR | Silicon Proc. for VLSI; 177-178; Vol. 1; S. Wolf | | | | |
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| EXAMINER | | | | DATE CONSIDERED | | |
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| | AQ | | Electronic Materials Science: For Integrated Circuits; 1990 ©; Mayer et al; pp. 269-274; Pub. 1990 | | | | |
| | AR | | Intrinsic Stress in Silicon Nitride and Silicon Dioxide Films Prepared by Various Deposition Techniques; 1988 IEEE Internatl. Sympos. On Electrical Insulation, Boston, MA; June 5-8, 1988; 1 page; Kanicki, J. et al. | | | | |
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